REMARKS

Claims 1-5 and 25-38 are pending in the application. Claims 1 and 33 are independent. By the foregoing Amendment, claims 1 and 33 have been amended. These changes are believed to introduce no new matter and their entry is respectfully requested.

Rejection of Claims 1-4 Under 35 U.S.C. §102(b)

In the Office Action, the Examiner rejected claims 1-4 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,203,613 to Gates et al. (hereinafter "*Gates*"). Applicant respectfully traverses the rejection.

A claim is anticipated only if each and every element of the claim is found, either expressly or inherently, in a reference. (MPEP §2131 *citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). The identical invention must be shown in as complete detail as is contained in the claim. Id. *citing Richardson v. Suzuki Motor Co.*, 868 F.2d 1226,1236 (Fed. Cir. 1989)).

Embodiments of the present invention are directed to preventing reaction of metal oxides with underlying silicon substrate during deposition of the metal oxide on the silicon substrate. One problem addressed by embodiments of the present invention is that deposition of metal oxides on silicon commonly results in the formation of silicon oxide or metal silicate at the interface between the metal oxide and the silicon substrate. Another problem is that the remaining bulk of the metal oxide film that is not in contact with the silicon substrate should have the high electrical insulation against current leakage desired in gate dielectrics. Conventional Atomic Layer Deposition (ALD) techniques do not achieve both elimination of interfacial oxide/silicate layers and high electrical insulation against current leakage. Instead, there is a tradeoff: accept oxide/silicate layers and benefit from high electrical insulation from leakage current or benefit from no oxide/silicate layers but low electrical insulation from leakage current.

Embodiments of the present invention may eliminate interfacial oxide/silicate layers as well as achieve high electrical insulation against current leakage desired in gate dielectrics.

Amended claim 1 recites in pertinent part "determining first properties of a metal oxide film to be disposed on a silicon substrate surface, the ***first properties of the metal oxide film to be determined by an interface between the silicon substrate surface and the metal oxide film***; establishing first atomic layer deposition (ALD) conditions for depositing the metal oxide film having the first properties on the silicon substrate surface; growing at least one monolayer of the metal oxide film having the first properties using the first ALD conditions; determining second properties of the metal oxide film to be disposed on the at least one monolayer, the ***second properties of the metal oxide film to be determined by a bulk portion of the metal oxide film***, the second properties being different from the first properties; establishing subsequent ALD conditions for depositing the metal oxide film having the second properties on the at least one monolayer; and growing at least one subsequent monolayer of the metal oxide film on the first monolayers using the subsequent ALD conditions" (emphasis added).

Applicant respectfully submits that *Gates* fails to disclose the identical invention as recited in claim 1. For example, *Gates* fails to disclose "first properties of the metal oxide film to be determined by an interface between the silicon substrate surface and the metal oxide film" as recited in claim 1. *Gates* also fails to disclose "second properties of the metal oxide film to be determined by a bulk portion of the metal oxide film" as recited in claim 1. *Gates* therefore fails to anticipate claim 1 and as a result claim 1 is patentable over *Gates*.

Claims 2-4 properly depend from claim 1. Accordingly, Applicant respectfully submits that claims 2-4 are patentable for at least the same reasons that claim 1 is patentable. (MPEP §2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 1-4.

Rejection of Claims 5 and 25-38 Under 35 U.S.C. §103(a)

In the Office Action, the Examiner rejected claims 5 and 25-38 under 35 U.S.C. §103(a) as being obvious over Gates in view of U.S. Patent Publication No. US 2002/0195056 to Sandhu et al. (hereinafter "*Sandhu*") in view of U.S. Patent Publication No. US 2005/0016956 to Liu et al. (hereinafter "*Liu*") in further view of U.S. Patent Publication No. US 2002/0144786 to Chiang et al. (hereinafter "*Chiang*"). Applicant respectfully traverses the rejection.

To establish a *prima facie* case of obviousness, an Examiner must show that there is some expectation of success that the combination proffered would result in the claimed invention. The Examiner also must show that the cited references teach each and every element of the claimed invention. (MPEP §2143.) *citing In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art. *KSR Int'l C. v. Teleflex, Inc.*, No 04-1350 (U.S. Apr. 30, 2007). It can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art elements in the manner claimed. However, an Examiner's reasoning that results in a change in the principle of operation of one or more references may not be used to render the claimed invention obvious. MPEP §2143.01 (citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)).

Amended claim 33 recites in pertinent part "determining first properties of a metal oxide film to be disposed on a silicon substrate surface, ***the first properties of the metal oxide film to be determined by an interface between the silicon substrate surface and the metal oxide film***; establishing first atomic layer deposition (ALD) conditions for depositing the metal oxide film having the first properties on the silicon substrate surface; running a first set of cycles in a reactor having the silicon substrate positioned therein using the first ALD conditions to grow at least one first monolayer of the metal oxide film, the at least one first monolayer having the first properties; determining subsequent properties of the metal oxide film to be disposed on the at least one monolayer, ***the subsequent properties of the metal oxide film to be determined by a bulk portion of the metal oxide film***, the second properties being different from the first properties; establishing subsequent ALD conditions for depositing the metal oxide film having the subsequent properties on the at least one monolayer; and running a subsequent set of cycles in the reactor using the subsequent ALD conditions to grow at least one subsequent monolayer of the metal oxide film, the at least one subsequent monolayer having subsequent properties different from the first properties" (emphasis added).

Applicant respectfully submits that *Gates* in view of *Sandhu* in view of *Liu*, in further view of *Chiang* fails to disclose each and every element of claim 33. As discussed above, *Gates* fails to disclose "first properties of the metal oxide film to be determined by an interface between

the silicon substrate surface and the metal oxide film" and fails to disclose "second properties of the metal oxide film to be determined by a bulk portion of the metal oxide film." Applicant respectfully submits that *Sandhu* fails to make up for this deficiency in *Gates*. *Sandhu* appears to be directed to eliminating problems associated with the batch processing, such as cross contamination of substrates from batch to batch and rector chamber wall contamination, by providing isolation between deposition processes using separated chambers. *Sandhu* is not concerned with the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film or concerned that the characteristics of the bulk film may need to be different from the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film.

Liu also fails to make up for this deficiency in *Gates* in view of *Sandhu*. *Liu* appears to be directed to reducing cycle times of ALD processes caused by long purge times needed to ensure uniformity of a deposited film. *Liu* is not concerned with the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film or concerned that the characteristics of the bulk film may need to be different from the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film.

Chiang also fails to make up for this deficiency in *Gates* in view of *Sandhu* in further view of Liu. *Chiang* appears to be directed to limitations of ALD reactors. *Chiang* is not concerned with the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film or concerned that the characteristics of the bulk film may need to be different from the characteristics of the film at the interface between the silicon substrate surface and the metal oxide film.

Thus Applicant respectfully submits that the combination of that *Gates* in view of *Sandhu* in view of *Liu*, in further view of *Chiang* fails to disclose "first properties of the metal oxide film to be determined by an interface between the silicon substrate surface and the metal oxide film" and fails to disclose "second properties of the metal oxide film to be determined by a bulk portion of the metal oxide film." Because the combination of that *Gates* in view of *Sandhu* in view of *Liu*, in further view of *Chiang* fails to disclose "first properties of the metal oxide film to be determined by an interface between the silicon substrate surface and the metal oxide film" and

fails to disclose "second properties of the metal oxide film to be determined by a bulk portion of the metal oxide film" the combination of that *Gates* in view of *Sandhu* in view of *Liu*, in further view of *Chiang* fails to disclose each and every element of claim 33 and as such claim 33 is patentable over the combination of that *Gates* in view of *Sandhu* in view of *Liu*, in further view of *Chiang*.

Claims 5 and 25-32 properly depends from claim 1. Accordingly, Applicant respectfully submits that claims 5 and 25-32 is patentable for at least the same reasons that claim 1 is patentable. (MPEP §2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 5 and 25-32.

Claims 34-38 properly depend from claim 33. Accordingly, Applicant respectfully submits that claims 34-38 are patentable for at least the same reasons that claim 33 is patentable. (MPEP §2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 33-38.

CONCLUSION

Applicant submits that all grounds for rejection have been properly traversed, accommodated, or rendered moot and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,
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